Kit386EXR

INDUSTRIAL CONTROL UNIT

Programmer and User Manual

Valid for printed circuit version 4

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SCT071

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Board Kit386EXR SCN071 sheet 0

1. Introduction

Kit386EXR is a small single-board computer, suitable for use as a universal control unit of industrial control systems, machines, apparatuses, regulators and data acquisition systems. Its core consists in a 32-bit processor I386EX, which is, with respect to programming, fully compatible with the Intel 80386(8086) processor. There are several interfaces for the connection of peripheral devices and extension modules:

- standard industrial bus - PC104;
- IO bus – IOBUS;
- binary inputs/outputs – PBUS;
- 2 asynchronous serial communication line channels with modem signals and the option of RS232 or a Com bus with TTL signals for the data part;
- or 1 synchronous communication line channel.

It is possible to connect various digital and analogue modules to these interfaces, extending the basic technical equipment and allowing the connection of many types of devices.

The board also includes an accurate real time clock, RAM, ROM, FLASH memory as an option, a battery and a Watch-Dog.

The Kit386EXR control board allows access to RAM and ROM by using an 8b or a 16b access. The 16b access is advantageous for time-intensive applications. Running an application written in a higher programming language on a system with 8b or 16b access only requires a different placement of the programme in the physical memory. If the Kit Builder language is used, all that is needed is to load the programme into the memory and activate it.

Kit386EXR has been designed for the firm's kit called KIT, in which it fully replaces the KitV40 control unit. The migration of applications from KitV40 to Kit386EXR only requires recompiling the programme with system libraries supporting the I386EX processor.

The following is offered for the control systems of the KIT kit: the Kit Builder – PLC Automat or ReTOS Debugger development tools, the ReTOS real time operating system and library functions in the PASCAL language for cooperation with the devices of other manufacturers such as protocol TECO, Lecom, SAIA and others.

For the KIT kit (Kit386EXR, KITV40, etc.), there are manuals describing the Kit Builder, ReTOS Debugger, MCP BIOS, ReTOS and there are also manuals for the supplied libraries.

This manual is valid for printed circuit board version **4.** The version can be identified from the label on the soldering side, where the last digit applies to the version of the printed circuit board. For example, for version **4**, the label SCB071 A-**4** is stated on the board.

2. Technical Description

This chapter will describe the main parts of the Kit386EXR board and the basic properties of the individual blocks; see **Fig.1**.

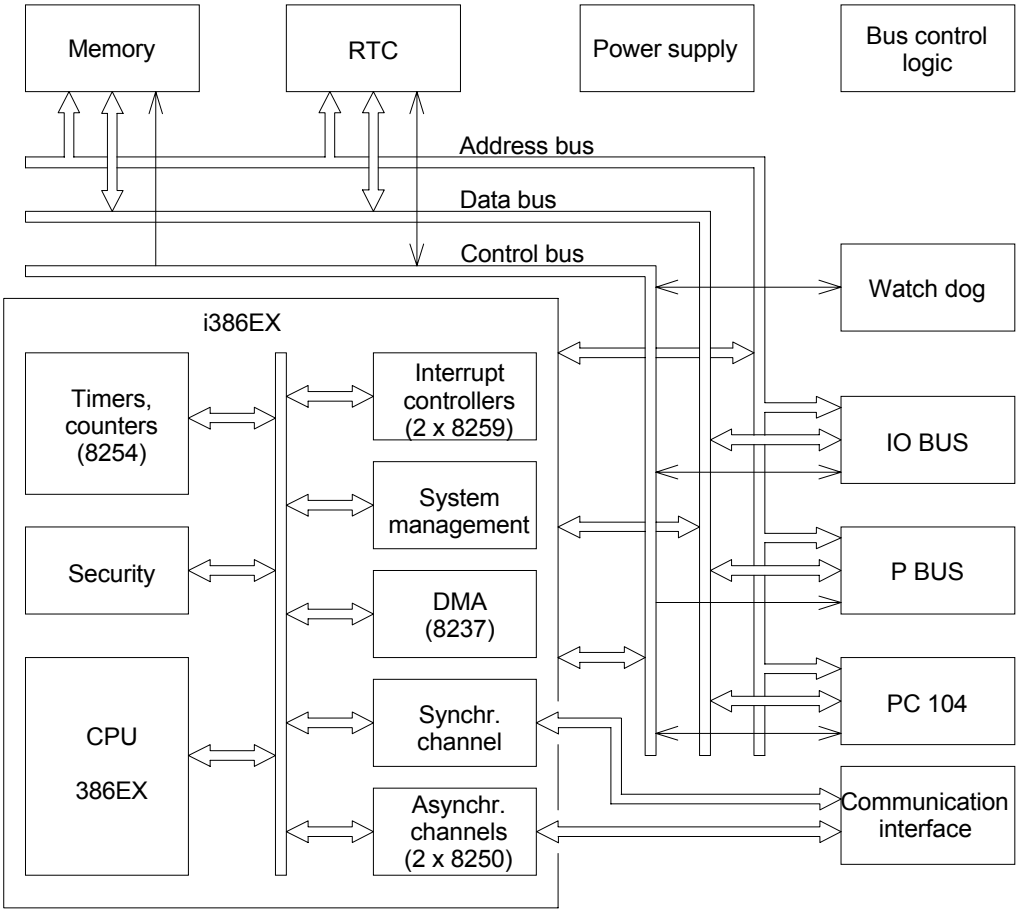


Fig. 1: Flow Chart of the Kit386EXR Board

2.1. Power Supply

The Kit386EXR control unit can be fed with low alternating or direct voltage; the values are stated in the Chapter titled “Basic Technical Data”. The connected input voltage is rectified and stabilised by using a power output pulse source.

2.2. Memory

The Kit386EXR unit can be equipped with EPROM, RAM and FLASH memory. A detailed description of the possibility of equipping individual sockets with the relevant components is contained in Table 5 and Table 6. The names of the individual sockets refer to Fig. 2 in Chapter 3.1.

The table also shows the possibilities of using the memories for various settings of the configuration table with the present software, where 1MB is available to the user and the remaining space is only accessible by using the delivered libraries creating RAM, FLASH and ROM disks. RAM is backed up with a battery.

Note: The abbreviation OM used in Tables Table 5 and Table 6 stands for Operating Memory.

2.3. Daily Clock - RTC

The RTC circuit, backed up with a battery, is used in the control unit for keeping accurate time. It keeps time to 1/64 of a second, seconds, minutes, hours, days, months and years. It can also be programmed as a wake-up alarm or as a source of interruption.

2.4. Supervisory – Watch-Dog

To ensure the correct operation of the control unit, a supervisory circuit is used, which is a combination of a monitor of the power supply voltage, RESET generator, power fail comparator and a Watch-Dog supervisory function.

- The monitor of the power supply voltage monitors the amplitude of the power supply voltage and if this drops below the level of 4.5 V – 4.75 V, it generates a RESET signal.
- The reset generator will ensure the correct duration of the RESET signal after the start of the power supply voltage.
- The power fail comparator monitors the voltage supplied to its input and if this is low, it generates a signal, which is transmitted to a non-maskable interrupt (NMI) of the I386EX processor.
- The Watch-Dog supervises the activities of the processor. The programme must change the level at the WDI input approximately every 1 s by reading the appropriate IO port. If this condition is not fulfilled, the RESET signal will be generated. This can be used to watch technical equipment as well as software because the generation of the setting pulse can depend upon the fulfilment of several different conditions.

This standard supervisory can also be supplemented with an internal Watch-Dog circuit of the I386EX processor; see “I386EX Processor” below.

2.5. Signalling

An LED diode is used to signal the operation of the processor. This diode is controlled by the signal, which is identical to the signal for setting the Watch-Dog security function. If the LED diode is required to be on permanently, it is necessary to generate a short setting pulse for the Watch-Dog function.

2.6. PC104 Industrial Bus

The PC104 bus has been designed for connection of the most complex peripheral devices:

- video boards;
- LCD adapters;
- adapters for PCMCIA (PC card);
- disk controllers;
- network boards;
- etc.

•

The following data, address and control signals lead to the interface:

D0..D15, A0..A23, IORD/, IOWR/, MEMR/, MEMW/, ALE, AEN/, DRQ1, DRQ2, DACK1, DACK2, IRQx, RESET, OSC , SYSCLK, REFRESH/, IOCS16/, MEMCS16/, IOCHRDY, OWS/(ENDXFR)

2.7. IOBUS

The IO bus is a firm's interface designed for the connection of extension IO modules. The IO modules may contain input and output registers, communication circuits, counters, timers, A/D and D/A converters, digital inputs and outputs, power components, etc.

The IO modules are installed on distance columns above or below the Kit386EXR control unit and are connected with a flat cable with connectors for ribbon cable. The terminal elements are installed at the end of the bus (the IOTERA or IOTERB board).

The following signals lead to the bus:

D0..D7, A0..A9, IRQ3, IRQ4, IOR/, IOW/, AEN/, RESET/

2.8. PBUS

The P bus is an interface designed for the connection of P modules, or it may be used as a normal parallel V/V. It contains three bidirectional eight-bit ports, A, B and C, whose directions can be switched over by programming. All outputs are provided with output drivers and when the control board is reset, they go into non-active status. It is possible to connect or disconnect them by writing a value to the appropriate address in the IO space. With output drivers, it is possible first to define their contents and only then can they be connected as outputs.

2.9. Communication Interface

The communication interface provides two asynchronous communication channels, which can be set as a COM bus with TTL signals or RS232 and/or alternatively as a synchronous channel interface with one asynchronous channel. Other modules, which considerably extend the usability of this interface, can be connected to the COM bus.

The following signals lead to the interface:

DCD/, RXD, TXD, DTR/, DSR/, RTS/, CTS/, RI/, GND, VCC, SRXCLK, STXCLK, SSIOTX, SSIORX

2.10. The I386EX Processor

The basic component of the Kit386EXR control unit is the I386EX processor by INTEL. The circuit contains a processor, which is fully compatible with the Intel 80386 processor with respect to programming, two i8259A interrupt controllers, an i8254counter/timer, two i8250 asynchronous communication circuits (with controlling signals), an extended i8237 DMA controller, etc.

- **Counters/Timers**

  In the I386EX processor, there is an i8254 circuit available. Counter 0 is used as a system timer and is transmitted to the i8259A interrupt controller. Counter 1 can be used as a timer for switching to a special mode referred to as System Management Mode (hereinafter referred to as "SMM"), for triggering DMA transmission, generating interruption at IRQ2 in another i8259A circuit, or it can be used for any desired purpose. Counter 2 can be used as a timer for generating interruption at IRQ3 in another i8259 circuit, or it can be used for any desired purpose.

- **Asynchronous Serial Channels**

  In the I386EX processor, there are two i8250 circuits with modem signals available. With both channels, for asynchronous communication data signals, it is possible to set the RS232 interface (the modem signals are on the TTL level), a Com bus (additional modules – RS485 or RS232 – can be connected to the interface) or to set an RS232 interface on a part of channel A for DCD/, DTR/ data signals and modem signals (possibility of interconnecting to the RTS signal using a jumper) and to set a Com bus interface on all of channel B.

- **Synchronous Serial Channel**

  On the second asynchronous communication channel, it is possible to set synchronous communication by using jumpers and setting specifications in the BIOS configuration.

- **DMA Channels**

  In the I386EX processor, there is an i8237 circuit available, which can only be used on the PC104 industrial bus. Unlike to PC AT, there are only 2 channels available on this bus; these channels are connected to channels 1 and 2 and are shared with COM2. This is why it is necessary to reconfigure the jumpers and set specifications in the BIOS configuration to activate them.

- **Interrupt Controllers**

  In the I386EX processor, there are two i8259A circuits available.
  The individual interrupt levels can be used as follows:
  - Level 0 is used for the system timer.
  - Level 1 is transmitted to the PC104 bus as INT1.
  - Level 2 is used for connection with another i8259A interrupt controller.
  - Level 3 is used for COM2.
  - Level 4 is used for COM1.
  - Level 5 is transmitted either to the PC104 bus as INT5 or to the IOBUS bus as INT3.
  - Level 6 is transmitted to the PC104 bus as INT6.
  - Level 7 is transmitted to the PC104 bus as INT7.
  - Level 8 is transmitted to the PC104 bus as INT8.
  - Level 9 is transmitted either to the PC104 bus as INT9 or to the IOBUS bus as INT4.
  - Level 10 can be used for timer 1.
  - Level 11 can be used for timer 2.
  - Level 12 can be used for interruption from DMA channels.
  - Level 13 is transmitted to the PC104 bus as INT13.
  - Level 14 is transmitted either to the PC104 as INT14 or to the real time clock (RTC) circuit.

- ## Supervisory the Processor

  The standard supervisory can be supplemented with a Watch-Dog internal circuit of the I386EX processor whose refresh interval corresponds to the value set in a 32b counter, whose clock frequency is derived from double the processor's clock frequency.

  ## System Management Mode

  The I386EX processor provides an additional interrupt level known as System Management Mode, hereinafter referred to as SMM. Table 1 provides an explanation of the interrupt priorities in the I386EX processor.

Interrupt level	Interruption name
1 (highest)	Double fault
2	Segmentation violation
3	Page fault
4	Divide by zero
5	SMM
6	Single step
7	Debug
8	ICE break
9	NMI
10	IRQ
11 (lowest)	I/O Lock

Table 1: Interrupt Priorities

Note: Certain interruptions are only available in the protected mode.

3. Configuration and Installation

3.1. Jumper Configuration

Fig. 2 shows the location of individual jumpers that can be used to set the properties of the KIT386EXR control unit. It is apparent from the figure that the individual jumpers are clustered into jumper fields and that these fields are named according to the property that they influence most strongly. The following chapters will refer to these names and will describe the selected jumper fields. In order to prevent confusion when a jumper field is connected, each field is identified with a key, which marks the number one or a unique point. This key is shown as a bold line.

With the sockets for ROM or RAM, there is always the word "**Low**" or "**High**". This description indicates the method of connecting the socket to the data bus. The prefix **Low** designates a connection to a D0-D7data bus; the prefix **High** designates a connection to a D8-D15 data bus. The memory on a higher data bus can only be used as a ROM disk, a FLASH disk or a RAM disk if there is 8b access. This is why the access type, memory size and jumper configuration will always be stated in the text below.

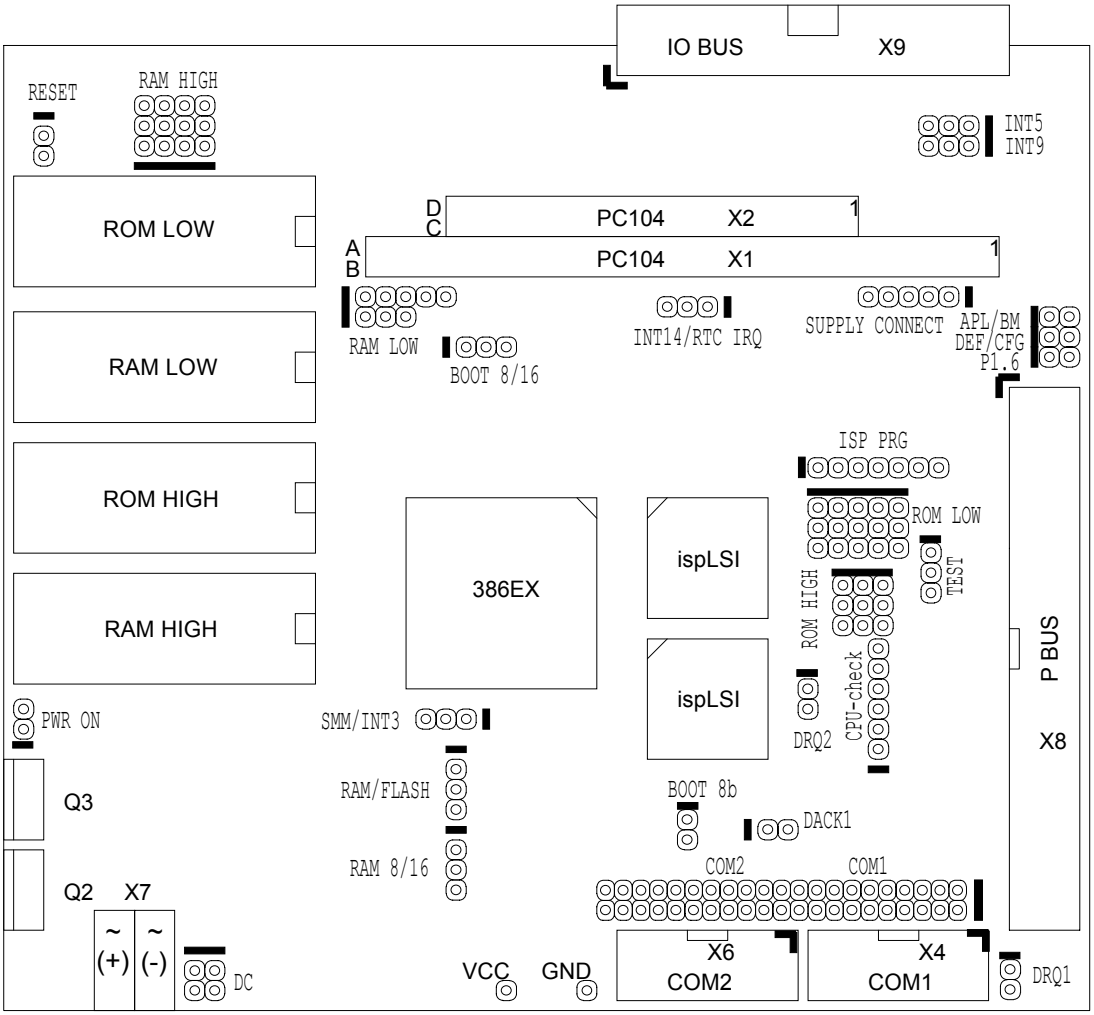


Fig. 2: Location of Jumpers on the KIT386EXR Board

Note: With jumpers where there are two possibilities of configuration, the function (property) applicable when the jumper is connected is always stated in the first

instance. If the name of the jumper does not contain a second configuration alternative, the name always applies to a connected jumper.
Note: It is advisable to make a copy of Fig. 2 and to draw the required configuration of the jumpers in this figure.

3.1.1. Setting Access to ROM and Specifications of ROM Low

By setting the BOOT ROM 8b and BOOT ROM 8/16 jumpers (see Fig. 4), you determine the access to the ROM into which the BIOS and the application programme are loaded, i.e. it is a selection from 8b and 16b access. Setting the access will significantly influence the speed of the programme execution; this is why a 16b access should be used for time-intensive applications.

When an 8b mode is set, the programme is executed in one ROM designated as ROM Low. This memory is divided into two parts by the lowest address bit A0 (see Fig. 3), which means that half of the programme is on odd addresses and the other half is on even addresses. The ROM Low is connected to the D0 – D7 data bus.

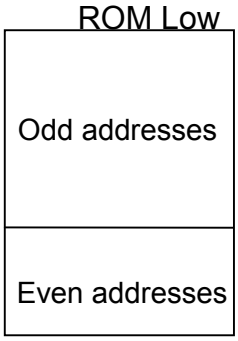


Fig. 3: Division of a Programme in 8b ROM

Note: The execution of one machine code instruction 2 bytes long in a memory with an 8b access requires at least 2 accesses against 1 access to ROM with 16b access.

When a 16b access is set, the programme is executed in two ROMs. The memory designated as ROM Low contains the part of the programme placed on even addresses, and the memory designated as ROM High contains the part placed on odd addresses; see.

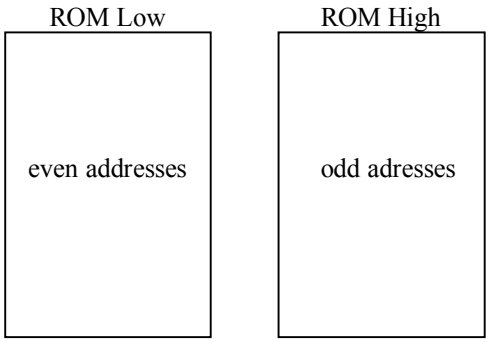


Fig. 4: Division of a Programme in a 16b ROM

The programme is divided by using the A0 address bit. ROM Low is connected to the D0-D7 data bus and ROM High is connected to the D8-D15 data bus.

In this mode, the sizes of both memories must be identical. The configuration of the specifications of ROM Low is shown in Fig. 4.

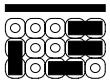
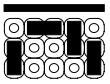
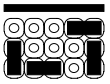
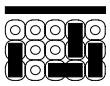
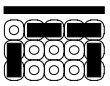
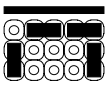
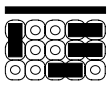
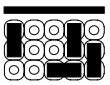
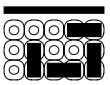
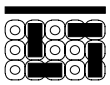
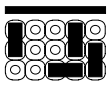
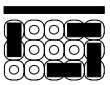
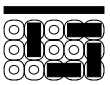
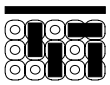
	ROM LOW				BOOT 8b	BOOT 8/16
	128k	256k	512k	1M		
FLASH 8 bit						
FLASH 16 bit						
EPROM 8 bit						
EPROM 16 bit						

Fig. 4: Setting the Access to ROM and the Specifications of ROM Low

3.1.2. Setting the Size of ROM High

The memory designated as ROM High can be used as a ROM disk, a FLASH disk for archived data, or as a programme memory. The use of this memory is determined particularly by the BOOT ROM 8b and BOOT ROM 8/16 jumpers. If a 16b access is set, the size of the memory in the ROM High socket must be the same as the size of the memory in the ROM Low socket. ROM High is connected to the D8-D15 data bus and with a 16b access, it contains the half of a programme stored on odd addresses.

The configuration of the specifications of ROM High is shown in Fig. 5.

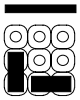
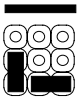
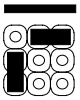
	ROM HIGH			
	128k	256k	512k	1M
EPROM				
FLASH				

Fig. 5: Setting the Size of ROM High

3.1.3. Setting the Access to RAM and the Specifications of RAM Low

Setting the RAM 8/16 and RAM/FLASH jumper (see Fig. 6 and Fig. 8) determines the access to RAM, i.e. the selection from an 8b and a 16b access. Setting the access will significantly influence the speed of the programme execution; this is why a 16b access should be used for time-intensive applications.

When an 8b mode is set, the data and variables are read from and written into a single RAM, designated as RAM Low. This memory is divided by the lowest A0 address bit into two parts (see Fig.), which means that half of the programme is on odd addresses and the other half is on even addresses. RAM Low is connected to the D0-D7 data bus.

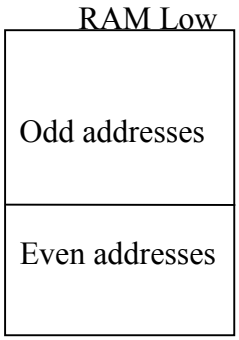


Fig. 7: Division of Programme Data in an 8b RAM

Note: Reading data 2 bytes long from, or writing data 2 bytes long to, a memory with an 8b access requires at least 2 accesses against 1 access to RAM with a 16b access.

When a 16b access is set, the data are placed in two RAMs. The memory designated as RAM Low contains the part of the data located on even addresses, and RAM High contains the part located on odd addresses; see 8. The data are divided by using the address bit A0. RAM Low is connected to the D0-D7 data bus and RAM High is connected to the D8-D15 data bus.

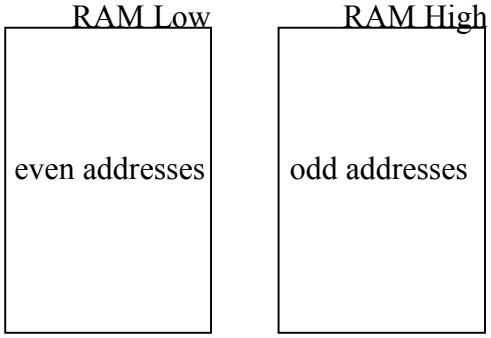


Fig. 8: Division of Programme Data in a 16b RAM

In this mode, the sizes of both memories must be identical. The configuration of RAM Low is shown in Fig. 6.

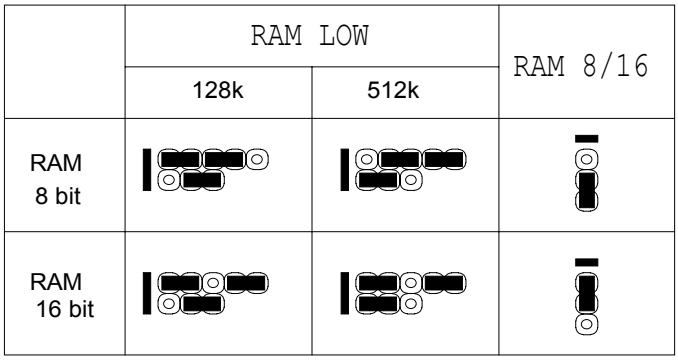


Fig. 6: Setting the Access to RAM and the Specifications of RAM Low

3.1.4. Setting the Size of RAM High

The memory designated as RAM High can be used as a RAM disk or a FLASH disk for archived data or for programme memory. The use of this memory is determined by the RAM 8/16 and the RAM/FLASH jumpers. If a 16b access is set, the size of the memory in the RAM High socket must be the same as the size of the memory in the RAM Low socket and the RAM/FLASH jumper must be set to the RAM HIGH Power on protection position. RAM High is connected to the D8-D15 data bus and with a 16b access, it contains the half of the programme (data) that is stored on odd addresses.

The configuration of the size of RAM High is shown in Fig. 7.

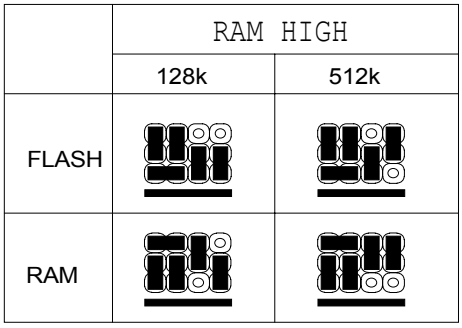


Fig. 7: Setting the Size of RAM High

When RAM is used in the RAM High socket, it is necessary to connect the protection of the contents of the RAM when the power supply is on by using the RAM/FLASH jumper; see Fig. 8. The jumper setting RAM High power on protection is designed particularly for a 16b access to a backed up RAM.

If this jumper is set to FLASH, then RAM can only be used in 8b access and the RAM High is used as a RAM disk whose contents will not be protected reliably. **We strongly recommend** that this setting should never be used.

In addition, if this jumper is connected incorrectly, the service life of the battery can be reduced significantly, especially if the contents of the FLASH memory are protected after the power supply is turned on. This is why the jumper must always be in the FLASH position when the FLASH memory is used.

	RAM/FLASH
RAM HIGH POWER ON PROTECTION	
FLASH	

Fig. 8: Setting the Protection of RAM High after the Power Supply Is On

3.1.5. Selecting the Connection of Shared Pins – DMA, COM2

Since certain COM2 pins are shared with the signals of the DMA channels, it is necessary to set the configuration in BIOS and the jumpers as shown in

	DRQ1	DACK1	DRQ2
COM2			
DMA1 + rest of COM2			
DMA2 + rest of COM2			
DMA1 + DMA2			

Fig. 9, if non-standard use is planned. The first column of the table always states the required function and selection of the DMA channel and the adjacent columns show the configuration of the jumpers. The COM2 function is set as a default; this configuration also applies to BIOS.

If DMA channels are to be used, the jumpers on the COM2 interface must also be set; see

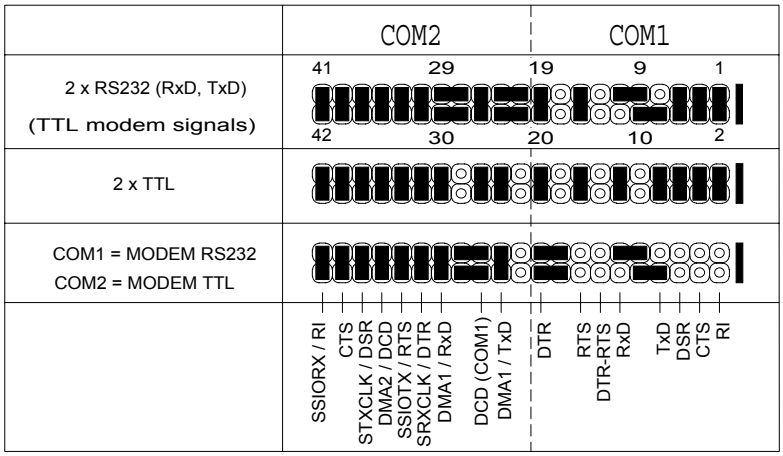


Fig. **13**. This picture, showing the COM1 and COM2 jumpers, indicates which COM2 signals are shared with the DMA channels. For these shared signals, the jumpers on COM2 must be removed in order to prevent a collision of signals. Otherwise, the remaining part of COM2 can only be used in the scope allowed by the remaining signals.

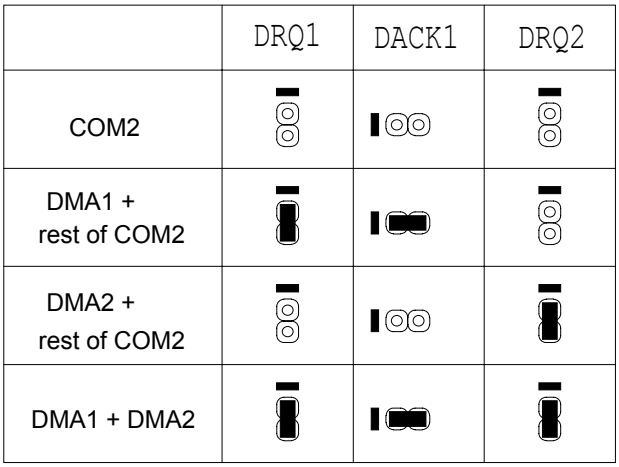


Fig. 9: Selection of DMA or COM2

3.1.6. Selecting Shared Pins – Synchronous Communication and COM2

With regard to the fact that the synchronous communication pins are shared with COM2, it is necessary to set the configuration in BIOS and the COM1 and COM2 jumpers, if synchronous communication is required. These jumpers are to be set as shown in

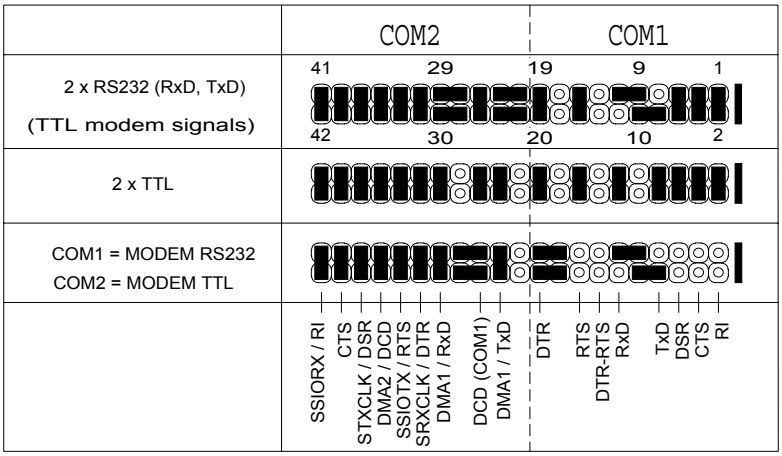


Fig. 13 in the TTL version for the COM2 channel.

The COM2 function is set as a default; the same setting also applies to BIOS.

3.1.7. Setting the INT5, INT9 and INT14 Sources of Interruption

Fig. 10 describes the setting of the INT5 and INT9 interruptions, where it is possible to choose either PC104 or IOBUS as the source of interruption. If IOBUS is set as the source of interruption, it is necessary to keep in mind that interruption INT3 at IOBUS is actually interruption INT5 and, similarly, INT4 at IOBUS is INT9.

Note: The designation INT at the CPU means an interruption corresponding to the interruption at the interrupt controllers, Master and Slave.

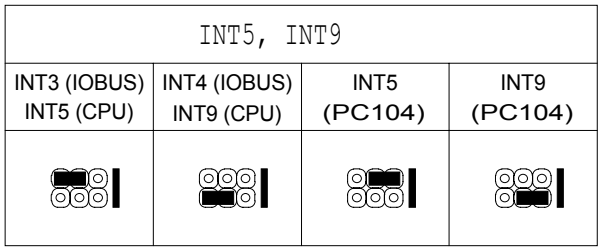


Fig. 10: Selection of the INT5 and INT9Interruption Sources

Fig. 11 shows a selection from PC104 or RTC as the source of interruption for INT14.

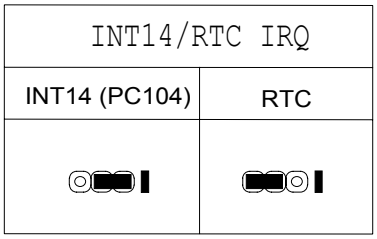


Fig. 11: Setting the Source of Interruption for INT14

3.1.8. Setting the SMM/INT3 Jumper

This jumper is not fitted as a standard and if an SA processor is installed, it can only be used as the timer output for switching to SMM. If a TC processor is installed, it can be used not only as the output of a timer for switching to SMM but also as an input of the INT3 interruption; see Fig. 12. If INT3 has been set, it is also necessary to make a change in the BIOS configuration by using RTD and to keep in mind what type of processor you are working with.

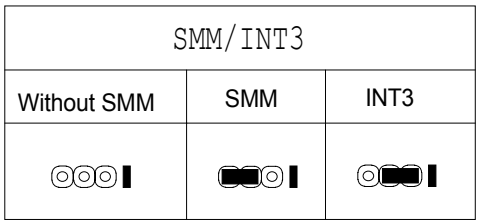


Fig. 12: Setting the SMI/INT3 Jumper

3.1.9. Setting the COM1 and COM2 Jumpers

This jumper field is used to choose whether the communication interface will be RS232 or a COM bus with TTL signals. By setting these jumpers, it is possible to achieve three basic interface options for both channels. There are two options in which both channels have the same interface, or there is an option (the last option) in which there is an interface dedicated to connection to a modem. These options are shown in

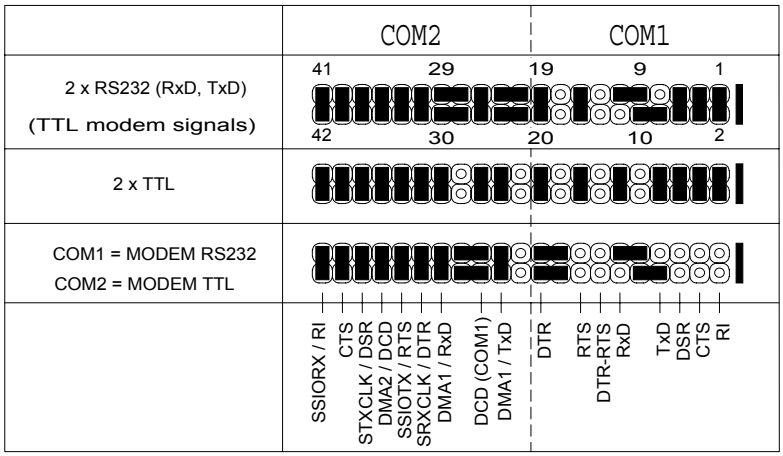


Fig. 13. If it is necessary to combine a COM bus and RS232, only the appropriate part of the picture will be used with regard to the channel to be set.

If DMA1 is to be used, the jumper on the signal RxD, TxD at COM2 must not be fitted, and if DMA2 is to be used, the jumper on DCD/ at COM2 must not be

fitted. The operation of COM2 is affected by the BIOS configuration; see the description of the configuration table in the Manual for BIOS386EXR.

Warning: Be careful of the signal DCD/; this signal belongs to the COM1 connector, while the jumper is found on the interface for COM2.

Note: With regard to the fact that the DTR and RTS signals cannot be concurrently and independently at the interface for direct modem connection, there is a DTR-RTS jumper in the jumper field. This jumper is used to combine the DTR and RTS signals. This jumper is fitted in a situation in which a modem requires the concurrent activation of both signals for complete initialisation.

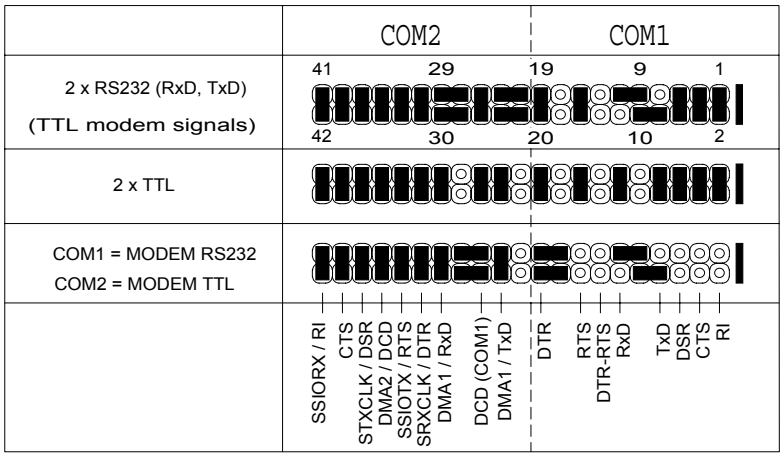


Fig. 13: Setting the COM1 and COM2 Jumpers

The block diagram showing the configuration of the COM1 and COM2 jumper field is shown in Fig. 14. The diagrammatic symbol of the operational amplifiers represents the converters with the levels 5V -> RS232 and RS232 -> 5V.

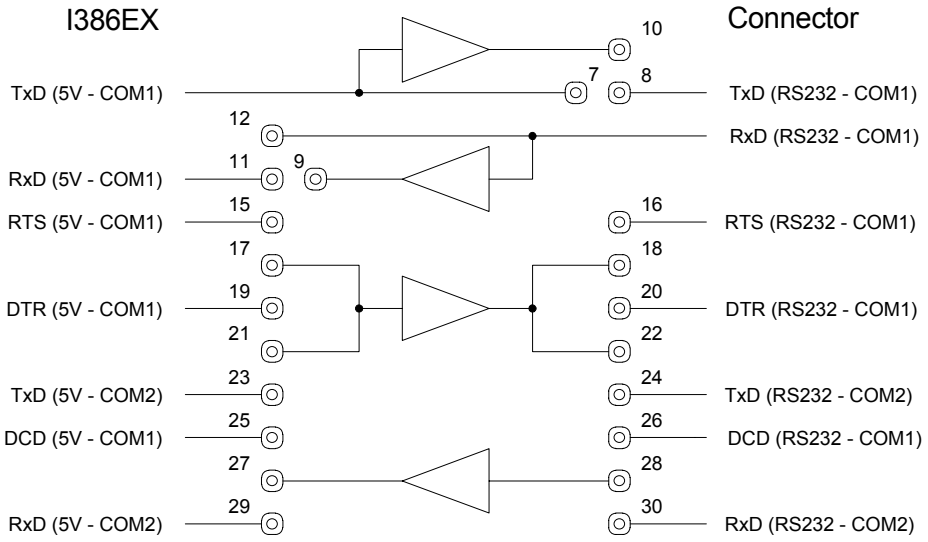


Fig. 14: Block Diagram of the Configuration of the COM1 and COM2 Jumper Field

3.1.10. The PWR ON Connector

The PWR ON connector is used to turn off the power supply of the Kit386EXR control board remotely. The power supply of the controlling voltage (from 2 to 7V) must deliver a minimum current of 3.5 mA. After the voltage is supplied as shown in Fig. 15, the power supply will be blocked and the control board will be turned off. The consumption of the board will drop below 3mA.

Warning: Be careful of the polarity of the connected power supply, as incorrect polarity may damage the power supply and the Kit386EXR board.

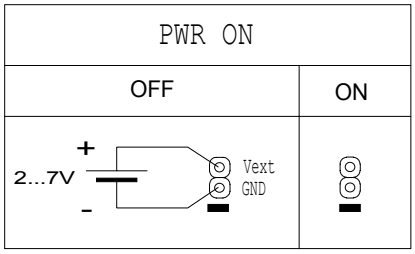


Fig. 15: Description of the PWR ON Connector

3.1.11. Setting the TEST Jumper

The TEST jumper is in the DEFAULT position as a standard and the second position is designed for servicing purposes.

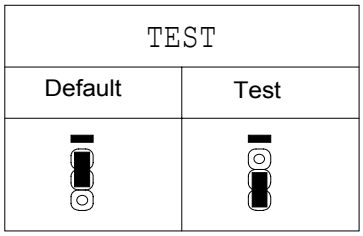


Fig. 16: Description of the TEST Jumper

3.1.12. Setting the Power Supply - DC

The DC jumper (see Fig. 17) is used to set the type of supply voltage. The DC setting is recommended when rectified voltage is used or when a battery is used as the power supply. This configuration will eliminate the potential of 0.7V between the extension boards and the control board. If DC is selected, it is necessary to make sure that the polarity of the power supply is as shown in Fig. 2. The AC/DS setting is used particularly in cases in which it is not known whether rectified or alternating voltage will be used in the application. The AC/DC option is set as a default.

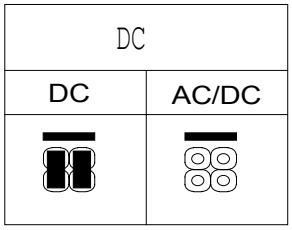


Fig. 17: Setting the Power Supply

3.1.13. Setting the Jumper Application/BIOS Monitor - APL/BM

When the jumper is set to the BIOS monitor position, the BIOS monitor is always started after initialisation of the control board. If the jumper is set to the Application position, the application programme will be started, if a LOADER unit is placed in RTD within the range of the absolute addresses 0C0000h-0FD000h and if the control board has been switched into ***CFG mode***. The ***Default Mode*** setting is only designed for making a change in the BIOS configuration.

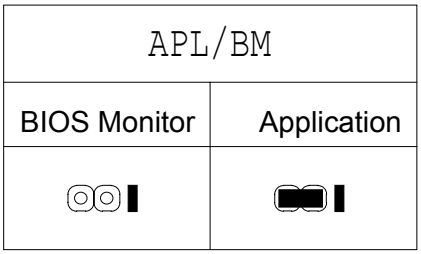


Fig. 18: Setting the Jumper Application/BIOS Monitor - APL/BM

3.1.14. Setting the Jumper Default/CFG Mode - DEF/CFG

If the jumper is set to the default position, the control board will be started in a mode that has been designed for making changes in the BIOS configuration. In this mode, the application is never started after initialisation of the control board; the BIOS monitor is always started.

If the jumper is set to the CFG position, the BIOS monitor will be started depending on the setting of the Application/BIOS monitor jumper. If there is an error in the configuration table, the control system may not work. If the system does not start due to an incorrect configuration setting, short-term operation will not damage the system; a long-term condition of this kind must never arise.

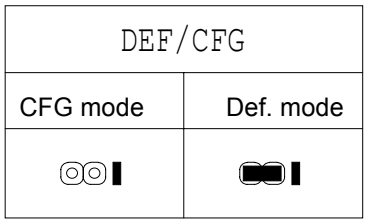


Fig. 19: Setting the Jumper for the Default/CFG mode - DEF/CFG

3.1.15. Jumper JP1.6

This jumper is reserved.

3.1.16. ISP PRG Connector

This connector is used for writing a programme into the programmable circuits when the board is finished during the production and/or when the firmware of the bus controllers is modified.

3.1.17. CPU-Check Connector

This connector is used for servicing and checking the functionality of the CPU during production.

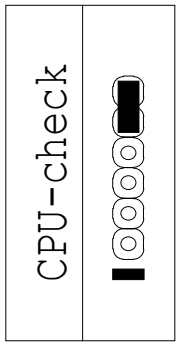


Fig. 20: CPU – Check connector

3.1.18. Supply Connector

This connector is for connection of voltages of +5V, -5V, +12V and –12V to the PC104 bus. The PC104 bus only has voltage of +5V as a standard and this connector is used for boards that require the above-mentioned voltages.

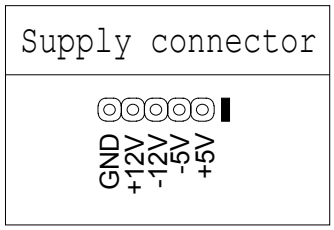


Fig. 21: Description of the Supply Connector

3.1.19. RESET Jumper

By using this jumper (see Fig. 22), the entire system can be brought into the initial state (RESET). For initialisation, it is necessary to connect the jumper for a period of at least 0.5 s. It is necessary to generate the RESET signal, for example, when working with an EPROM memory simulator or when working with a FLASH memory.

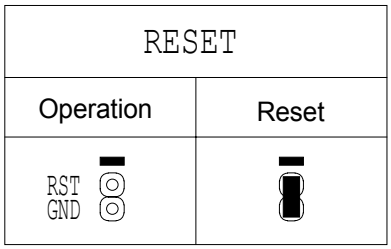


Fig. 22: Description of the RESET Jumper

The RESET jumper can be controlled by an external switch such as that shown in Fig. 23. The voltage between RST and GND must be lower than 1V and the switch must be able to transmit a minimum of 3mA.

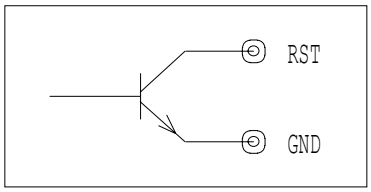


Fig. 23: Description of RESET External Control

3.2. Description of Jumper Settings

This section will describe the procedure for making decisions on configuring the Kit386EXR control board. The manual will always state what we want to influence and what jumper field must be set so that the control board works as you desire.

Required configuration, change or status of the control board	Set or check the jumper field given below
• access to ROM	BOOT ROM 8/16, BOOT ROM 8b, ROM Low, ROM High
• ROM size	ROM Low, ROM High
• using FLASH memory instead of EPROM or EPROM instead of FLASH	ROM Low, ROM High
• access to RAM	RAM 8/16, RAM/FLASH, RAM Low, RAM High
• RAM size	RAM Low, RAM High
• using FLASH memory in the position of RAM High	RAM 8/16, RAM/FLASH, RAM High
• it is not possible to measure +5V on the board	DC
• BIOS is not started (LED does not blink on Kit386EXR – in this case, it is necessary to switch it to Default Mode by using Default/CFG Mode)	RESET, BOOT ROM 8/16, BOOT ROM 8b, ROM Low, ROM High, RAM 8/16, RAM Low, RAM High, CPU - Check connector
• application is not started after RESET	DEF/CFG - Default/CFG mode, APL/BM - Application/BIOS monitor
• interruption does not work at the IOBUS bus	INT5, INT9

3.3. Connecting the Connectors

3.3.1. Connecting the Power Supply

The power supply voltage defined in the “Operational Conditions” chapter is connected to the X7 connector. When the DC jumper is being set, it is necessary to make sure that the polarity of the voltage is as shown in Fig. 17.

3.3.2. Connecting the IO Modules

The modules designed for IOBUS are connected to the X8 connector. The number of modules is determined by the input current of the individual modules. The modules are connected by using a flat cable with a PFL34 connector for ribbon cable.

3.3.3. Connecting the P Modules

The modules designed for PBUS are connected to the X9 connector. The number of modules is determined by the input current of the individual modules. The modules are connected by using a flat cable with a PFL50 connector for ribbon cable.

4. Overview of the Memory Address Space

Address space	Meaning			
00000-7FFFF	RAM (HEX)			RAM
	00000	**-**	**003FF**	Interrupt vectors
	00400	**-**	**004FF**	BIOS data
	00500	**-**	**0050F**	Print screen
	00600	**-**	**0063F**	Serial communication
	00640	**-**	**0177F**	BIOS monitor
	01780	**-**	**03FFF**	BIOS monitor buffer
	04000	**-**	**7FFFF**	Area of RAM (for programme memory, the memory from the 00B0h address can be used)
80000-FFFFF	ROM (HEX)			ROM
	80000	**-**	**9FFFF**	Area of ROM
	A0000	**-**	**BFFFF**	Area of VIDEO RAM
	C0000	**-**	**C7FFF**	Area of VIDEO BIOS
	C8000	**-**	**FCFFF**	Area of ROM
	FD000	**-**	**FFFFF**	Area of BIOS

Table 2: Overview of Memory Use in Kit386EXR

**) The RAM area can be placed from the $000B0 address only upon the condition that STACK, DATA Segment and HEAP are placed in this memory. The area for backed up data must always start higher than $04000.

5. Overview of the Constants in BIOS

Address (HEX)	Meaning	
FFF00	**word**	***Configuration table*** The value describing the properties of the U3 socket, Base 1, ROM Low
FFF02	**word**	***Configuration table*** The value describing the properties of the U4 socket, Base 2, RAM Low
FFF04	**word**	***Configuration table*** The value describing the properties of the U6 socket, Base 3, ROM High
FFF06	**word**	***Configuration table*** The value describing the properties of the U7 socket, Base 4, RAM High
FFF08	**word**	***Configuration table*** The beginning and size of ROM High
FFF09	**byte**	***Configuration table*** The beginning and size of extended BIOS systems
FFF0A	**byte**	***Configuration table*** The beginning and size of ROM Low
FFF0B	**word**	***Configuration table*** Configuration setting
FFF0D	**word**	Constants for CPU detection
FFF0F	**word**	Constants for CPU detection
FFF11	**word**	Constants for CPU detection
FFF13	**word**	Constants for CPU detection
FFF15	**word**	Constants for CPU detection
FFF17	**word**	Constants for CPU detection
FFF19	**word**	REMAPCFG initialisation value
FFF1B	**word**	PINCFG initialisation value
FFF1D	**word**	DMACFG initialisation value
FFF1F	**word**	INTCFG initialisation value
FFF21	**word**	TMRCFG initialisation value
FFF23	**word**	SIOCFG initialisation value
FFF25	**word**	RFSCIR initialisation value
FFF27	**word**	RFSBAD initialisation value
FFF29	**word**	RFSADD initialisation value
FFF2B	**word**	RFSCON initialisation value
FFF2D	**word**	PORT92 initialisation value
FFF2F	**word**	PWRCON initialisation value
FFF31	**word**	CLKPRS initialisation value
FFFCC	**word**	Offset of the space where the string describing the BIOS is stored
FFFCE	**word**	Segment where the string describing the BIOS is stored
FFFD0	**word**	Memory size in Kbyte, see Int 12h
FFFD2	**word**	System configuration, see Int 11h
FFFD4	**word**	Initial segment for search for extension BIOS systems
FFFD6	**word**	SP reg. BIOS initialisation value
FFFD8	**word**	SS reg. BIOS initialisation value
FFFDA	**word**	Initialisation value of the transmission speed of the BIOS monitor

Table 3: Overview of the Constants in the MCP BIOS of the Kit386EXR Control Board

6. Overview of the V/V Address Space

6.1. IO Space

Address space (HEX)			Meaning
0000 **0080**	**-** **-**	**000F** **0090**	18271 DMA controller of the I386EX processor
0020	**-**	**0021**	18259A interrupt controller of the I386EX processor
0022	**-**	**0022**	REMAPCFG address configuration register
0040	**-**	**0043**	18254 timer, counter of the I386EX processor
0092	**-**	**0092**	A20GATE and FastCPU Reset
00A0	**-**	**00A1**	18259A interrupt controller of the I386EX processor
02F8	**-**	**02FF**	18251 UART of the I386EX processor
03F8	**-**	**03FF**	18251 UART of the I386EX processor
2000	**-**	**23FF**	IOBUS, R/W
4000	**-**	**43FF even address**	WDI function Watch-Dog and the LED diode is on. Note: With regard to future development, it is recommended to use the 4210h address.
4000	**-**	**43FF odd address**	Automatic operation of Watch-Dog and the LED diode is on. Automatic operation of Watch-Dog that is switched on in BIOS due to initialisation of the CRT controller. After having been switched off, it cannot be switched on again. Note: With regard to future development, it is recommended to use the 4211h address.
6000	**-**	**63FF**	WDI function Watch-Dog and the LED diode is on. Note: With regard to future development, it is recommended to use the 6210h address.
8000	**-**	**83FF**	RTC daily time clock, R/W. Note: With regard to future development, it is recommended to use the 8210h address.
D000	**-**	**D3FF**	Pbus, R/W Note: With regard to future development, it is recommended to use the D210h address.
F000	**-**	**F8FF**	Registers of I386EX (synchronous unit, refresh, watch-dog, clock generation, power management and parallel port configuration register)
xxxx	**-**	**xxxx**	The IO space not described here is reserved for PC104. This IO space also includes the unoccupied space between the registers of the CPU and the registers of the said peripheral devices.

Table 4: Occupation of the IO Space

6.2. PBus

The text below describes the individual ports at the PBUS interface. The value of 0D210h is recommended as the base address.

address	**meaning**
base+0	portA, R/W
base+1	portB, R/W
base+2	portC, R/W
base+3	setting port A to output, W
base+4	setting port A to input, W
base+5	setting port B to output, W
base+6	setting port B to input, W
base+7	setting port C to output, W
base+8	setting port C to input, W

7. Allocation of Signals to Connectors

7.1. PC104 Industrial Bus

X1 connector

B1	GND	A1	IOCHCK/ (not connected)
B2	RESET	A2	D7
B3	+5V	A3	D6
B4	IRQ9	A4	D5
B5	-5V (JP26 connector)	A5	D4
B6	DREQ2	A6	D3
B7	-12V (JP26 connector)	A7	D2
B8	OWS/ (ENDXFR/)	A8	D1
B9	+12V (JP26 connector)	A9	D0
B10	KEY	A10	IOCHRDY
B11	SMEMW/	A11	AEN
B12	SMEMR/	A12	A19
B13	IOW/	A13	A18
B14	IOR/	A14	A17
B15	DACK3/ (pull-out resistor)	A15	A16
B16	DREQ3 (not connected)	A16	A15
B17	DACK1/	A17	A14
B18	DREQ1	A18	A13
B19	REFSH/	A19	A12
B20	SYSCLK	A20	A11
B21	IRQ7	A21	A10
B22	IRQ8	A22	A9
B23	IRQ5	A23	A8
B24	IRQ4	A24	A7
B25	IRQ3	A25	A6
B26	DACK2/	A26	A5
B27	TC (not connected)	A27	A4
B28	BALE	A28	A3
B29	+5V	A29	A2
B30	OSC	A30	A1
B31	GND	A31	A0
B32	GND	A32	GND

X2 connector

D0	GND	C0	GND
D1	MEMCS16/	C1	SBHE/
D2	IOCS16/	C2	A23
D3	IRQ10	C3	A22
D4	IRQ11	C4	A21
D5	IRQ12	C5	A20
D6	IRQ15	C6	A19
D7	IRQ14	C7	A18
D8	DACK0/ (pull-out resistor)	C8	A17
D9	DRQ0	C9	MEMR/
D10	DACK5/ (pull-out resistor)	C10	MEMW/
D11	DRQ5	C11	D8
D12	DACK6/ (pull-out resistor)	C12	D9
D13	DRQ6	C13	D10
D14	DACK7/ (pull-out resistor)	C14	D11
D15	DRQ7	C15	D12
D16	+5V	C16	D13
D17	MASTER/ (not connected)	C17	D14
D18	GND	C18	D15
D19	GND	C19	KEY

7.2. IOBUS

X9 connector

1	VCC	2	VCC
3	VCC	4	VCC
5	IODAT0	6	IODAT1
7	IODAT2	8	IODAT7
9	IODAT6	10	IODAT5
11	IODAT4	12	IODAT3
13	IOADR0	14	AEN/
15	IOADR1	16	IOADR8
17	IOADR2	18	IOADR9
19	IOADR3	20	IOADR4
21	IOADR5	22	IOADR6
23	IOADR7	24	GND
25	INT 3 (connected to IRQ5)	26	GND
27	INT 4 (connected to IRQ9)	28	GND
29	IOWR/	30	GND
31	IORD/	32	GND
33	RESET/	34	GND

7.3. PBUS

X8 connector

1	PA0	2	GND
3	PA1	4	GND
5	PA2	6	GND
7	PA3	8	GND
9	PA4	10	GND
11	PA5	12	GND
13	PA6	14	GND
15	PA7	16	GND
17	PC0	18	GND
19	PC1	20	GND
21	PC2	22	GND
23	PC3	24	GND
25	PC4	26	GND
27	PC5	28	GND
29	PC6	30	GND
31	PC7	32	GND
33	PB0	34	GND
35	PB1	36	GND
37	PB2	38	GND
39	PB3	40	GND
41	PB4	42	GND
43	PB5	44	GND
45	PB6	46	GND
47	PB7	48	GND
49	VCC	50	VCC

7.4. Com bus

X4 connector

1	DCD/	2	DSR/
3	RxD	4	RTS/
5	TxD	6	CTS/
7	DTR/	8	RI/
9	GND	10	VCC

X6 connector

1	DCD/ (DMA2)	2	DSR/ (STXCLK)
3	RxD (DMA1)	4	RTS/ (SSIOTX)
6	TxD (DMA1)	6	CTS/
7	DTR/ (SRXCLK)	8	RI/ (SSIORX)
9	GND	10	VCC

8. Basic Technical Data

8.1. Operational Conditions

Operation	Uninterrupted
Power supply	From a supply of low safe voltage (PELV) as defined in ČSN 33 2000-4 Direct voltage of 10 through 35 Vss, including ripple or alternating voltage of 10 to 24 Vst, 50 to 60 Hz Recommended protection with a T3.15A/250V blow-out fuse
Environment	Industrial, not air conditioned, without aggressive gases or vapours
EMC	Emissions as defined in ČSN EN 50 081-2, Resistance as defined in ČSN EN 61000-6-2
Operating temperature	0°C to 70°C
Relative humidity	35 to 85% at 25°C
Atmospheric pressure	86 to 107kPa
Working vibrations	max. 0.15 mm at 55 Hz

8.2. Technical Specifications

Dimensions	122 x 138 x 25 mm, the board can be mounted into assembly frames on DIN/EN TS 32 and TS 35 strips.
Storage temperature	-10°C to 80°C
Weight	0,17kg
Coverage	IP 00
Supply current without extension modules	maximum 350 mA at 10Vss; maximum 150 mA at 35Vss
Permitted load of the 5V supply output	1.4A (standard version) 2.7A (version with additional cooling apparatus)
Processor	INTEL 386 EX, 33(25) MHz (80386 SX + 2 x 8259 + 8254 + 2 x 8250 + 8237A+..)

Memory

In the basic version, there is 256kB EPROM, 128 kB RAM.
The memory capacity can be extended up to the following maximum sizes (MB):

EPROM	FLASH	RAM	Total MB
2x1	-	2x0.5	3
2x1	1x0.5	1x0.5	3
1x1	1x0.5	2x0.5	2.5
1x1	2x0.5	1x0.5	2.5
-	2x0.5	2x0.5	2
-	3x0.5	1x0.5	2

Interface

asynchronous serial communication

2 channels with the choice of RS232 or Com BUS (TTL) with a maximum speed of 115KBd (COM1, COM2)

synchronous serial communication

optionally, 1 channel instead of COM2 with a maximum speed of 6.25MBd at 25MHz

IOBUS

X9 connector – 34 pin

max. I_{OL} 20mA
max. I_{OH} -20mA
max. I_{IL} 1uA
min. V_{IH} 3.5V
max. V_{IL} 1.5V

The address drivers are shared with the PC104 bus.

PBUS

X8 connector – 50 pin

max. I_{OL} 20mA
max. I_{OH} -20mA
max. I_{IL} 1uA
min. V_{IH} 2.0V
max. V_{IL} 0.8V

All outputs are provided with output drivers and when the control board is reset they achieve a third status. Their connection is possible by writing a value to the appropriate address in the V/V space.

Keyboard

A keyboard can be connected to COM2 by using a PCKB module.

PC104

X2 connector – 120 pin and X1 – 132 pin.
Values for address signals, data signals and output control signals:

max. I_{OL}	20mA
max. I_{OH}	-20mA
max. I_{IL}	1uA
min. V_{IH}	2.0V
max. V_{IL}	0.8V

The address drivers are shared with IOBUS.
Values for input control signals:

max. I_L	±15uA
min. V_{IH}	3.5 V (SA) 2V (TC)
max. V_{IL}	1.5V (SA) 0.8V (TC)

Pull-out resistors:

interrupt signals	2k2
data signals	4k7
xWR/,xRD/, BHE/, xCS16/	4k7

The signals with the note *pull-out resistors* at connectors X1 and X2 are connected through 4k7 to Vcc.

9. Ordering

The following is to be specified in an order:
type and size of RAM and ROM (EPROM/FLASH)
type of access to RAM and ROM (8b/16b)

Example of an order:
RAM 512kB - 8b access
FLASH 512kB - 16b access

The connectors, cables, the PCKB module for keyboard connection, the VGA card for the PC104 bus, the extension I/O modules from the KIT kit and the PC104 bus can be supplied on the basis of a special order.

Access	ROM Low	ROM High	Possibilities of use [kB]						
8b	EPROM/FLASH 128kB	Unfitted	OM	16	32	64	128		
			ROM disk	112	96	64	0		
			FLASH disk	112	96	64	0		
	EPROM/FLASH 256kB	Unfitted	OM	16	32	64	128	256	
			ROM disk	240	224	192	128	0	
			FLASH disk	240	224	192	128	0	
	EPROM/FLASH 512kB	Unfitted	OM	16	32	64	128	256	512
			ROM disk	496	480	448	384	256	0
			FLASH disk	496	480	448	384	256	0
	EPROM 1024kB	Unfitted	OM	16	32	64	128	256	512
			ROM disk	1008	992	960	896	768	512
	Setting with the above-mentioned combinations	EPROM/FLASH 128kB EPROM/FLASH 256kB EPROM/FLASH 512B EPROM 1024kB	With an 8b access, ROM High is reserved for a ROM disk or a FLASH disk. The values of the OM correspond to the values stated above, depending on the fitted memory in ROM Low. The sizes of the disks change depending on the size of the memory fitted in ROM High.						
16b	EPROM/FLASH 128kB	EPROM/FLASH 128kB	OM	16	32	64	128	256	
			ROM disk	240	224	192	128	0	
			FLASH disk	240	224	192	128	0	
	EPROM/FLASH 256kB	EPROM/FLASH 256kB	OM	16	32	64	128	256	512
			ROM disk	496	480	448	384	256	0
			FLASH disk	496	480	448	384	256	0
	EPROM/FLASH 512kB	EPROM/FLASH 512kB	OM	16	32	64	128	256	512
			ROM disk	1016	992	960	896	768	512
			FLASH disk	1016	992	960	896	768	512
	EPROM 1024kB	EPROM 1024kB	OM	16	32	64	128	256	512
			ROM disk	2032	2016	1984	1920	1792	1536

Table 5: Possibilities of Setting the Board with ROM Low and ROM High

Access	RAM Low	RAM High	Possibilities of use [kB]						
8b	RAM 128kB	Unfitted	OP	16	32	64	128		
			RAM disk	112	96	64	0		
	RAM 512kB	Unfitted	OP	16	32	64	128	256	512
			RAM disk	496	480	448	384	256	0
	Setting with the above-mentioned combinations	RAM/FLASH 128kB RAM/FLASH 512kB	With an 8b access, RAM High is reserved for a RAM disk or a FLASH disk. The sizes of OM correspond to the values stated above depending on the fitted RAM Low. The sizes and types of the disks change depending on the fitted RAM High. If a RAM disk is used, it is more advantageous to use a 16b access.						
16b	RAM 128kB	RAM 128kB	OP	16	32	64	128	256	
			RAM disk	240	224	192	128	0	
	RAM 512kB	RAM 512kB	OP	16	32	64	128	256	512
			RAM disk	1016	992	960	896	768	512

Table 6: Possibilities of Setting the Board with RAM Low and RAM High